AMENDMENT TO THE CLAIMS

Please amend the claims as follows:

1-2. (Cancelled)

3. (Previously presented) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a general purpose register used for an arithmetic operation of a CPU and having a function of receiving, delivering and storing data, the general purpose register having a data unit;

a secure information unit included in the general purpose register and adapted to be set to a state not requiring security in a case that the data is transferred from the user memory space to the data unit of the general purpose register, and adapted to be set to a state requiring security in a case that the data is transferred from the secure memory space to the data unit of the general purpose register;

a data control unit having a function of determining whether a value of the secure information unit is in the state requiring security or the state not requiring security when the data of the general purpose register is written in the user memory space, thereby determining whether a data transfer to the user memory space is prohibited or not;

an address control unit having a function of determining which of the user memory space and the secure memory space is indicated by an address information, and selecting the value of the secure information unit;

a user program arranged in the user memory space;

a secure program arranged in the secure memory space;

an instruction fetch address control unit having a function of determining which of the user memory space and the secure memory space is indicated by the address information when storing an instruction code input from the data control unit, and a function of notifying the data control unit which of the user program and the secure program is under execution;

an instruction buffer used by the CPU to fetch the instruction code and having a function of storing therein the instruction code input from the data control unit;

a plurality of the general purpose registers and a plurality of the secure information units included in each of the general purpose registers, respectively, the secure information units further being capable of being set to a state of invalid security, and

a general purpose register file, the general purpose register file is configured to set, when performing the arithmetic operations between at least two of the general purpose registers in compliance with an operating instruction, the value of the secure information unit of the general purpose registers to which a result of the arithmetic operation is stored to the state of invalid security, if at least one of the values of the secure information unit indicates that the general purpose register having the state requiring security is operated, wherein:

when the data control unit issues the operating instruction to the general purpose register with the secure information unit having the state of invalid security, the data control unit prohibits the arithmetic operation, if the instruction fetch address control unit determines that the operating instruction has been fetched from the user memory space, and

when the data control unit executes the data transfer from the data unit of the general purpose register to the memory spaces in compliance with a transfer instruction, the data transfer to the user memory space is prohibited, if the instruction fetch address control unit determines

that the instruction code is fetched from the user memory space and the value of the secure information unit indicates the state requiring security.

4. (Previously presented) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a general purpose register used for an arithmetic operation of a CPU and having a function of receiving, delivering and storing data, the general purpose register having a data unit;

a secure information unit included in the general purpose register and adapted to be set to a state not requiring security in a case that the data is transferred from the user memory space to the data unit of the general purpose register, and adapted to be set to a state requiring security in a case that the data is transferred from the secure memory space to the data unit of the general purpose register;

a data control unit having a function of determining whether a value of the secure information unit is in the state requiring security or the state not requiring security when the data of the general purpose register is written in the user memory space, thereby determining whether a data transfer to the user memory space is prohibited or not;

an address control unit having a function of determining which of the user memory space and the secure memory space is indicated by an address information, and selecting the value of the secure information unit;

a user program arranged in the user memory space;

a secure program arranged in the secure memory space;

an instruction fetch address control unit having a function of determining which of the user memory space and the secure memory space is indicated by the address information when

storing an instruction code input from the data control unit, and a function of notifying the data control unit which of the user program and the secure program is under execution; and

an instruction buffer used by the CPU to fetch the instruction code and having a function of storing therein the instruction code input from the data control unit; and

a status register used for the arithmetic operation of the CPU and having a function of holding a value of a result of a comparative arithmetic operation as a comparative flag, the status register further having a function of keeping a value of each comparative flag unchanged, when the arithmetic operation is executed between at least two of the general purpose registers in compliance with an operating instruction, if at least one of the general purpose registers indicates the state requiring security and the instruction fetch address control unit determines that the operating instruction has been fetched from the user memory space, wherein:

when the data control unit executes the data transfer from the data unit of the general purpose register to the memory spaces in compliance with a transfer instruction, the data transfer to the user memory space is prohibited, if the instruction fetch address control unit determines that the instruction code is fetched from the user memory space and the value of the secure information unit indicates the state requiring security.

5. (Previously presented) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a general purpose register used for an arithmetic operation of a CPU and having a function of receiving, delivering and storing data, the general purpose register having a data unit;

a secure information unit included in the general purpose register and adapted to be set to a state not requiring security in a case that the data is transferred from the user memory space to

the data unit of the general purpose register, and adapted to be set to a state requiring security in a case that the data is transferred from the secure memory space to the data unit of the general purpose register;

a data control unit having a function of determining whether a value of the secure information unit is in the state requiring security or the state not requiring security when the data of the general purpose register is written in the user memory space, thereby determining whether a data transfer to the user memory space is prohibited or not;

an address control unit having a function of determining which of the user memory space and the secure memory space is indicated by an address information, and selecting the value of the secure information unit;

a user program arranged in the user memory space;

a secure program arranged in the secure memory space;

an instruction fetch address control unit having a function of determining which of the user memory space and the secure memory space is indicated by the address information when storing an instruction code input from the data control unit, and a function of notifying the data control unit which of the user program and the secure program is under execution;

an instruction buffer used by the CPU to fetch the instruction code and having a function of storing therein the instruction code input from the data control unit;

a read/write user IO space used for accessing the user memory space from outside; and

a read/write secure IO space used for accessing the secure memory space from outside, wherein:

the information processing apparatus is configured to receive an IC card connectable to the secure IO space and having a function of storing data, the IC card further including a debug

key configured to stop, when read out by the CPU through the secure IO space when a developer debugs the secure program with a user system, an address determining function ~~of~~ performed by the instruction fetch address control unit and the address control unit,

when the data control unit executes the data transfer from the data unit of the general purpose register to the memory spaces in compliance with a transfer instruction, the data transfer to the user memory space is prohibited, if the instruction fetch address control unit determines that the instruction code is fetched from the user memory space and the value of the secure information unit indicates the state requiring security, and

when transferring the data from the data unit of the general purpose register to the memory spaces in compliance with the transfer instruction, the data control unit permits the data transfer to the user memory space regardless the instruction code is fetched either from the user memory space or the secure memory space, if the debug key is read by the CPU.

6. (Currently amended) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a secure bit generating unit for receiving data and determining which of the user memory space and the secure memory space is indicated by address information associated with the received data, adding a secure bit to the received data based on determining which of the user memory space and the secure memory space is indicated by the address information associated with the received data, and delivering the received data with ~~one or more secure bits~~ the secure bit into a general purpose register [[with]] including a secure bit unit, the general purpose register having a function of receiving and holding the data with ~~one or more secure bits~~ the secure bit added thereto;

a built-in RAM space for receiving and holding the data with ~~one or more secure bits~~ the secure bit from the general purpose register and delivering the data with ~~one or more secure bits~~ the secure bit to the general purpose register; and

a data output control unit having a function of controlling a data transfer to an external space by using the secure bit;

wherein the data output control unit performs a control operation to determine whether the data transfer to the external space is prohibited or not by a value of the secure [[bits]] bit set in the general purpose register.

7. (Currently amended) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a secure bit generating unit for receiving data and determining which of the user memory space and the secure memory space is indicated by address information associated with the received data, adding a secure bit to the received data based on determining which of the user memory space and the secure memory space is indicated by the address information associated with the received data, [[and]] delivering the received data with ~~one or more secure bits~~ the secure bit into a general purpose register [[with]] including a secure bit unit, the general purpose register having a function of receiving and holding the data with ~~one or more secure bits~~ the secure bit added thereto, and delivering an instruction with ~~one or more secure bits~~ a secure bit into an instruction decoder [[with]] including a secure bit unit, the instruction decoder having a function of determining which of the user memory space and the secure memory space is associated with the instruction under execution;

a built-in RAM space [[with]] including a secure bit unit, the built-in RAM space for receiving and holding the data with ~~one or more secure bits~~ the secure bit from the general purpose register and delivering the data with ~~one or more secure bits~~ the secure bit to the general purpose register;

an interrupt saved information unit [[with]] including a secure bit unit, the interrupt saved information unit having a function of adding, upon generation of an interrupt process, the secure bit of the instruction decoder to data saved in a stack area of the built-in RAM space; and

a data output control unit having a function of controlling a data transfer to an external space by using the secure bit;

wherein the data output control unit performs a control operation to determine whether the data transfer to the external space is prohibited or not by a value of the secure [[bits]] bit set in the general purpose register.

8. (Currently amended) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a secure bit generating unit for receiving data and determining which of the user memory space and the secure memory space is indicated by address information associated with the received data, adding a secure bit to the received data based on determining which of the user memory space and the secure memory space is indicated by the address information associated with the received data, [[and]] delivering the received data with ~~one or more secure bits~~ the secure bit into a general purpose register [[with]] including a secure bit unit, the general purpose register having a function of receiving and holding the data with ~~one or more secure bits~~ the secure bit added thereto, and delivering an instruction with ~~one or more secure bits~~ a secure bit

into an instruction decoder [[with]] including a secure bit unit, the instruction decoder having a function of determining which of the user memory space and the secure memory space is associated with the instruction under execution;

a built-in RAM space [[with]] including a secure bit unit, the built-in RAM space having a function of receiving and holding the data with ~~one or more secure bits~~ the secure bit from the general purpose register and delivering the data with ~~one or more secure bits~~ the secure bit to the general purpose register;

an interrupt saved information unit [[with]] including a secure bit unit, the interrupt saved information unit having a function of adding, upon generation of an interrupt process, the secure bit of the instruction decoder to data saved in a stack area of the built-in RAM space;

a stack pointer for defining a part of the built-in RAM space as the stack area; and

a saved information rewrite control unit for controlling a rewrite operation in the stack area of the built-in RAM space;

wherein the saved information rewrite control unit prohibits the rewrite operation if the instruction of the instruction decoder is associated with the user memory space and intended to rewrite the stack area of the built-in RAM space.

9. (Currently amended) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a direct memory access unit (DMA) [[with]] including a secure bit unit having a function of holding ~~one or more secure bits~~ a secure bit;

a secure bit generating unit for receiving data and determining which of the user memory space and the secure memory space is indicated by address information associated with the

received data, adding a secure bit to the received data based on determining which of the user memory space and the secure memory space is indicated by the address information associated with the received data, and delivering the received data with ~~one or more secure bits~~ the secure bit into the DMA;

a built-in RAM space for receiving and holding the data with ~~one or more secure bits~~ the secure bit from the DMA and delivering the data with ~~one or more secure bits~~ the secure bit to the DMA; and

a data output control unit having a function of controlling a data transfer to an external space by using the secure bit,

wherein the data output control unit performs a control operation to determine whether the data transfer to the external space is prohibited or not by a value of the secure [[bits]] bit set in the DMA.

10. (Currently amended) An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a secure bit generating unit for receiving data and determining which of the user memory space and the secure memory space is indicated by address information associated with the received data, adding a secure bit to the received data based on determining which of the user memory space and the secure memory space is indicated by the address information associated with the received data, [[and]] delivering the received data with ~~one or more secure bits~~ the secure bit into a general purpose register [[with]] including a secure bit unit, the general purpose register having a function of receiving and holding the data with ~~one or more secure bits~~ the secure bit added thereto, and delivering an instruction with ~~one or more secure bits~~ a secure bit

into an instruction decoder [[with]] including a secure bit unit, the instruction decoder having a function of determining which of the user memory space and the secure memory space is associated with the instruction under execution;

an operating unit [[with]] including a secure bit unit having a function of reflecting the secure [[bits]] bit of the instruction decoder in an arithmetic operation executed in accordance with the instruction decoded by the instruction decoder; and

a data output control unit having a function of controlling a data transfer to an external space by using the secure bit,

wherein the data output control unit performs a control operation to determine whether the data transfer to the external space is prohibited or not by the secure bit set in the general purpose register and the secure bit set in the operating unit.

11. (Previously presented) The information processing apparatus according to claim 3, wherein

the user program is accessible mainly by a user, and

the secure program is accessible mainly by a developer and contents of the secure program is not disclosed to the user.

12. (Previously presented) The information processing apparatus according to claim 3, wherein the data control unit determines whether the data transfer to the user memory space is prohibited or not irrespective of a mode associated with a CPU.

13. (Previously Presented) The information processing apparatus according to claim 12, wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode.

14. (Previously presented) The information processing apparatus according to claim 6, wherein the data control unit determines whether the data transfer to the external space is prohibited or not irrespective of a mode associated with a CPU.

15. (Previously Presented) The information processing apparatus according to claim 14, wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode.

16. (Previously presented) The information processing apparatus according to claim 7, wherein the data control unit determines whether the data transfer to the external space is prohibited or not irrespective of a mode associated with a CPU.

17. (Previously Presented) The information processing apparatus according to claim 16, wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode.

18. (Previously presented) The information processing apparatus according to claim 9, wherein the data control unit determines whether the data transfer to the external space is prohibited or not irrespective of a mode associated with a CPU.

19. (Previously Presented) The information processing apparatus according to claim 18, wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode.

20. (Currently amended) The information processing apparatus according to claim 8, wherein the data control unit determines whether the data transfer to the external space is prohibited or not irrespective of [[the]] a mode associated with a CPU.

21. (Previously Presented) The information processing apparatus according to claim 20, wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode.

22. (New) The information processing apparatus according to claim 6, wherein adding the secure bit to the received data includes:

adding a first value to the received data based on determining that the user memory space is indicated by the address information associated with the received data, and

adding a second value to the received data based on determining that the secure memory space is indicated by the address information associated with the received data.

23. (New) The information processing apparatus according to claim 7, wherein adding the secure bit to the received data includes:

adding a first value to the received data based on determining that the user memory space is indicated by the address information associated with the received data, and

adding a second value to the received data based on determining that the secure memory space is indicated by the address information associated with the received data.

24. (New) The information processing apparatus according to claim 8, wherein adding the secure bit to the received data includes:

adding a first value to the received data based on determining that the user memory space is indicated by the address information associated with the received data, and

adding a second value to the received data based on determining that the secure memory space is indicated by the address information associated with the received data.

25. (New) The information processing apparatus according to claim 9, wherein adding the secure bit to the received data includes:

adding a first value to the received data based on determining that the user memory space is indicated by the address information associated with the received data, and

adding a second value to the received data based on determining that the secure memory space is indicated by the address information associated with the received data.

26. (New) The information processing apparatus according to claim 10, wherein adding the secure bit to the received data includes:

adding a first value to the received data based on determining that the user memory space is indicated by the address information associated with the received data, and

adding a second value to the received data based on determining that the secure memory space is indicated by the address information associated with the received data.